



AMENDMENTS TO THE CLAIMS:

Please cancel without prejudice claims 2, 3, 14, 15, 26, 27, 38, 39, 50, 51, 62, 63, 73, 74, 85 and 86, amend claims 1, 13, 25, 37, 49, 61, 72 and 84 and add newly written claims 96-111 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A data processing apparatus comprising:

a master device;

a first slave device; and

a common communication bus providing a plurality of communication paths between said master device, said first slave device and at least one further slave device, and for passing transaction requests from said master device to said first slave device; wherein

said master device having a transaction annotator for generating a transaction identifier as part of each transaction request passed from said master device to said first slave device, said transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request; and

said first slave device having transaction ordering logic operable to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers, wherein said master identifier portion specifies one of a plurality of possible master identifier values associated with said master device, wherein said transaction



ordering constraints relate only to subsets of transaction requests generated by said master device for which said master identifier portion specifies an identical master identifier value.

2. (cancelled).

3. (cancelled).

4. (original) A data processing apparatus according to claim 1, in which said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

5. (original) A data processing apparatus according to claim 1, in which said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier.

6. (original) A data processing apparatus according to claim 5, in which said timeout value is derived from concatenated values of at least part of said master identifier portion and said priority portion of said transaction identifier.

7. (previously presented) A data processing apparatus according to claim 6, in which said first slave device comprises logic operable to select a subset of bits of said master identifier

portion to be concatenated with said priority portion of said transaction identifier to derive said timeout value.

8. (original) A data processing apparatus according to claim 1, in which said priority request portion comprises at least one bit value specifying either a high priority or a low priority for a transaction request associated with said transaction identifier.

9. (previously presented) A data processing apparatus according to claim 1, in which said transaction request is either a read request for reading data from a memory attached to said first slave device or a write request for writing data to said memory attached to said first slave device.

10. (previously presented) A data processing apparatus according to claim 1, in which said transaction identifier comprises a sequence of bit values and said first slave device is programmable to apply a mask to said transaction identifier determining which of said sequence bit values correspond to said priority portion and which of said sequence of bit values correspond to said master identifier portion.

11. (previously presented) A data processing apparatus according to claim 1, in which said first slave device is a memory controller.

12. (original) A data processing apparatus according to claim 1, in which said master device is one of:

a central processing unit;

a direct memory access controller;
a liquid crystal display controller; or
a video accelerator.

13. (currently amended) A master device operable to pass transaction requests across a common communication bus to a first slave device, said master device for providing a plurality of communication paths between said master device, said first slave device and at least one further slave device, said master device comprising a transaction annotator for generating a transaction identifier as part of each transaction request passed from said master device to said first slave device, said transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request;

wherein said transaction identifier contains information enabling said first slave device to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from said master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers, wherein said master identifier portion specifies one of a plurality of possible master identifier values associated with said master device, wherein said transaction ordering constraints relate only to subsets of transaction requests generated by said master device for which said master identifier portion specifies an identical master identifier value.

14. (cancelled).

15. (cancelled).

16. (original) A master device according to claim 13, in which said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

17. (original) A master device according to claim 13, in which said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier.

18. (original) A master device according to claim 17, in which said timeout value is derived from concatenated values of at least part of said master identifier portion and said priority portion of said transaction identifier.

19. (previously presented) A master device according to claim 18, in which said first slave device comprises logic operable to select a subset of bits of said master identifier portion to be concatenated with said priority portion to derive said timeout value.

20. (original) A master device according to claim 13, in which said priority request portion comprises at least one bit value specifying either a high priority or a low priority for a transaction request associated with said transaction identifier.

21.(previously presented) A master device according to claim 13, in which said transaction request is either a read request for reading data from a memory attached to said first slave device or a write request for writing data to said memory attached to said first slave device.

22. (previously presented) A master device according to claim 13, in which said transaction identifier comprises a sequence of bit values and said first slave device is programmable to apply a mask to said transaction identifier determining which of said sequence bit values correspond to said priority portion and which of said sequence of bit values correspond to said master identifier portion.

23. (previously presented) A master device according to claim 13, in which said first slave device is a memory controller.

24. (original) A master device according to claim 13, in which said master device is one of:

- a central processing unit;
- a direct memory access controller;
- a liquid crystal display controller; or
- a video accelerator.

25. (currently amended) A first slave device operable to receive transaction requests from a master device across a common communication bus providing a plurality of communication paths between said master device, said first slave device and at least one further slave device,

said first slave device having transaction ordering logic operable process a transaction identifier received from a master device as part of a transaction request, said transaction request having a master identifier portion and a priority request portion specifying a priority value for said transaction request, said transaction ordering logic being operable to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from said master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers, wherein said master identifier portion specifies one of a plurality of possible master identifier values associated with said master device, wherein said transaction ordering constraints relate only to subsets of transaction requests generated by said master device for which said master identifier portion specifies an identical master identifier value.

26. (cancelled).

27. (cancelled).

28. (previously presented) A first slave device according to claim 25, in which said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

29. (previously presented) A first slave device according to claim 25, in which said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier.

30. (previously presented) A first slave device according to claim 25, in which said timeout value is derived from concatenated values of at least part of said master identifier portions and said priority portions of said transaction identifiers.

31. (previously presented) A first slave device according to claim 30, comprising logic operable to select a subset of bits of said master identifier portion to be concatenated with said priority portion of said transaction identifier to derive said timeout value.

32. (previously presented) A first slave device according to claim 25, in which said priority request portion comprises at least one bit value specifying either a high priority or a low priority for a transaction request associated with said transaction identifier.

33. (previously presented) A first slave device according to claim 25, in which said transaction request is either a read request for reading data from a memory attached to said first slave device or a write request for writing data to said memory attached to said first slave device.

34. (previously presented) A first slave device according to claim 25, in which said transaction identifier comprises a sequence of bit values and said first slave device is programmable to apply a mask to said transaction identifier determining which of said sequence

bit values correspond to said priority portion and which of said sequence of bit values correspond to said master identifier portion.

35. (previously presented) A first slave device according to claim 25, in which said first slave device is a memory controller.

36. (previously presented) A first slave device according to claim 25, in which said master device is one of:

- a central processing unit;
- a direct memory access controller;
- a liquid crystal display controller; or
- a video accelerator.

37. (currently amended) A common bus carrying a transaction request signal from a master device to a first slave device, said common bus providing a plurality of communication paths between said master device, said first slave device and at least one further slave device, and for passing said transaction request signal comprising a transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request, said transaction identifier enabling said first slave device to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers, wherein said master identifier portion specifies one of a plurality of

possible master identifier values associated with said master device, wherein said transaction ordering constraints relate only to subsets of transaction requests generated by said master device for which said master identifier portion specifies an identical master identifier value.

38. (cancelled).

39. (cancelled).

40. (original) A bus according to claim 37, in which said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

41. (original) A bus according to claim 37, in which said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier.

42. (original) A bus according to claim 41, in which said timeout value is derived from concatenated values of at least part of said master identifier portion and said priority portion of said transaction identifier.

43. (previously presented) A bus according to claim 42, in which said timeout value is derived by said first slave device using logic to select a subset of bits of said master identifier portion to be concatenated with said priority portion to derive said timeout value.

44. (original) A bus according to claim 37, in which said priority request portion comprises at least one bit value specifying either a high priority or a low priority for a transaction request associated with said transaction identifier.

45. (previously presented) A bus according to claim 37, in which said transaction request is either a read request for reading data from a memory attached to said first slave device or a write request for writing data to said memory attached to said first slave device.

46. (previously presented) A bus according to claim 37, in which said transaction identifier comprises a sequence of bit values and said first slave device is programmable to apply a mask to said transaction identifier determining which of said sequence bit values correspond to said priority portion and which of said sequence of bit values correspond to said master identifier portion.

47. (previously presented) A bus according to claim 37, in which said first slave device is a memory controller.

48. (original) A bus according to claim 37, in which said master device is one of:

a central processing unit;

a direct memory access controller;

a liquid crystal display controller; or

a video accelerator.

49. (currently amended) A data processing method for passing transaction requests from a master device to a slave device across a common communication bus providing a plurality of communication paths between said master device, said first slave device and at least one further slave device, said method comprising the steps of:

generating in a master device a transaction identifier as part of each transaction request passed from said master device to said first slave device, said transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request; and

determining at said first slave device an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers, wherein said master identifier portion specifies one of a plurality of possible master identifier values associated with said master device, wherein said transaction ordering constraints relate only to subsets of transaction requests generated by said master device for which said master identifier portion specifies an identical master identifier value.

50. (cancelled).

51. (cancelled).

52. (original) A data processing method according to claim 49, in which said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

53. (original) A data processing method according to claim 49, in which said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier..

54. (original) A data processing method according to claim 53, in which said timeout value is derived from concatenated values of at least part of said master identifier portions and said priority portions of said transaction identifiers.

55. (previously presented) A data processing method according to claim 54, in which said first slave device comprises logic operable to select a subset of bits of said master identifier portion to be concatenated with said priority portion of said transaction identifier to derive said timeout value.

56. (original) A data processing method according to claim 49, in which said priority request portion comprises at least one bit value specifying either a high priority or a low priority for a transaction request associated with said transaction identifier.

57. (previously presented) A data processing method according to claim 49, in which said transaction request is either a read request for reading data from a memory attached to said first slave device or a write request for writing data to said memory attached to said first slave device.

58. (previously presented) A data processing method according to claim 49, in which said transaction identifier comprises a sequence of bit values and said first slave device is programmable to apply a mask to said transaction identifier determining which of said sequence bit values correspond to said priority portion and which of said sequence of bit values correspond to said master identifier portion.

59. (previously presented) A data processing method according to claim 49, in which said first slave device is a memory controller.

60. (original) A data processing method according to claim 49, in which said master device is one of:

- a central processing unit;
- a direct memory access controller;
- a liquid crystal display controller; or
- a video accelerator.

61. (currently amended) A method of generating in a master device, transaction requests for sending across a common communication bus to a first slave device, said common

communications bus providing a plurality of communication paths between said master device, said first slave device and at least one further slave device, said method comprising the step of :

generating a transaction identifier as part of each transaction request passed from said master device to said first slave device, said transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request;

wherein said transaction identifier contains information enabling said first slave device to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from said master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers, wherein said master identifier portion specifies one of a plurality of possible master identifier values associated with said master device, wherein said transaction ordering constraints relate only to subsets of transaction requests generated by said master device for which said master identifier portion specifies an identical master identifier value.

62. (cancelled).

63. (cancelled).

64. (original) A method according to claim 61, in which said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

65. (original) A method according to claim 61, in which said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier.

66. (original) A method according to claim 65, in which said timeout value is derived from concatenated values of at least part of said master identifier portion and said priority portion of said transaction identifier.

67. (original) A method according to claim 61, in which said priority request portion comprises at least one bit value specifying either a high priority or a low priority for a transaction request associated with said transaction identifier.

68. (previously presented) A method according to claim 61, in which said transaction request is either a read request for reading data from a memory attached to said first slave device or a write request for writing data to said memory attached to said first slave device.

69. (previously presented) A method according to claim 61, in which said transaction identifier comprises a sequence of bit values and said first slave device is programmable to apply a mask to said transaction identifier determining which of said sequence bit values correspond to said priority portion and which of said sequence of bit values correspond to said master identifier portion.

70. (previously presented) A method according to claim 61, in which said first slave device is a memory controller.

71. (original) A method according to claim 61, in which said master device is one of:
a central processing unit;
a direct memory access controller;
a liquid crystal display controller; or
a video accelerator.

72. (currently amended) A method of controlling a slave device to service transaction requests received from a master device across a common communication bus providing a plurality of communication paths between said master device, said first slave device and at least one further slave device, said method comprising the step of:

processing a transaction identifier received from a master device as part of a transaction request, said transaction request having a master identifier portion and a priority request portion specifying a priority value for said transaction request, said transaction ordering logic being operable to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from said master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers, wherein said master identifier portion specifies one of a plurality of possible master identifier values associated with said master device, wherein said transaction ordering constraints relate only to subsets of transaction requests

generated by said master device for which said master identifier portion specifies an identical master identifier value.

73. (cancelled).

74. (cancelled).

75. (original) A method according to claim 72, in which said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

76. (original) A method according to claim 72, in which said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier.

77. (original) A method according to claim 76, in which said timeout value is derived from concatenated values of at least part of said master identifier portions and said priority portions of said transaction identifiers.

78. (previously presented) A method according to claim 77, in which said first slave device comprises logic operable to select a subset of bits of said master identifier portion to be concatenated with said priority portion of said transaction identifier to derive said timeout value.

79. (original) A method according to claim 72, in which said priority request portion comprises at least one bit value specifying either a high priority or a low priority for a transaction request associated with said transaction identifier.

80. (previously presented) A method according to claim 72, in which said transaction request is either a read request for reading data from a memory attached to said first slave device or a write request for writing data to said memory attached to said first slave device.

81. (previously presented) A method according to claim 72, in which said transaction identifier comprises a sequence of bit values and said first slave device is programmable to apply a mask to said transaction identifier determining which of said sequence bit values correspond to said priority portion and which of said sequence of bit values correspond to said master identifier portion.

82. (previously presented) A method according to claim 72, in which said first slave device is a memory controller.

83. (original) A method according to claim 72, in which said master device is one of:
a central processing unit;
a direct memory access controller;
a liquid crystal display controller; or
a video accelerator.

84. (currently amended) A method of transmitting a transaction request on a common communications bus providing a plurality of communication paths between a master device, a first slave device and at least one further slave device comprising the steps of:

generating a transaction request signal comprising a transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request, said transaction identifier enabling said first slave device to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers; and

transmitting said transaction request signal across said common communication bus, wherein said master identifier portion specifies one of a plurality of possible master identifier values associated with said master device, wherein said transaction ordering constraints relate only to subsets of transaction requests generated by said master device for which said master identifier portion specifies an identical master identifier value.

85. (cancelled).

86. (cancelled).

87. (original) A method according to claim 84, in which said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated

with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

88. (original) A method according to claim 84, in which said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier.

89. (original) A method according to claim 84, in which said timeout value is derived from concatenated values of at least part of said master identifier portions and said priority portions of said transaction identifiers.

90. (previously presented) A method according to claim 89, in which said first slave device comprises logic operable to select a subset of bits of said master identifier portion to be concatenated with said priority portion of said transaction identifier to derive said timeout value.

91. (original) A method according to claim 84, in which said priority request portion comprises at least one bit value specifying either a high priority or a low priority for a transaction request associated with said transaction identifier.

92. (previously presented) A method according to claim 84, in which said transaction request is either a read request for reading data from a memory attached to said first slave device or a write request for writing data to said memory attached to said first slave device.

93. (previously presented) A method according to claim 84, in which said transaction identifier comprises a sequence of bit values and said first slave device is programmable to apply a mask to said transaction identifier determining which of said sequence bit values correspond to said priority portion and which of said sequence of bit values correspond to said master identifier portion.

94. (previously presented) A method according to claim 84, in which said first slave device is a memory controller.

95. (original) A method according to claim 84, in which said master device is one of:
a central processing unit;
a direct memory access controller;
a liquid crystal display controller; or
a video accelerator.

96. (new) A data processing apparatus comprising:
a master device;
a first slave device; and
a common communication bus providing a plurality of communication paths between said master device, said first slave device and at least one further slave device, and for passing transaction requests from said master device to said first slave device; wherein
said master device having a transaction annotator for generating a transaction identifier as part of each transaction request passed from said master device to said first slave device, said

transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request; and

said first slave device having transaction ordering logic operable to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers, wherein said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

97. (new) A data processing apparatus comprising:

a master device;

a first slave device; and

a common communication bus providing a plurality of communication paths between said master device, said first slave device and at least one further slave device, and for passing transaction requests from said master device to said first slave device; wherein

said master device having a transaction annotator for generating a transaction identifier as part of each transaction request passed from said master device to said first slave device, said transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request; and

said first slave device having transaction ordering logic operable to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from master identifier

portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers, wherein said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier, wherein said timeout value is derived from concatenated values of at least part of said master identifier portion and said priority portion of said transaction identifier.

98. (new) A master device operable to pass transaction requests across a common communication bus to a first slave device, said master device for providing a plurality of communication paths between said master device, said first slave device and at least one further slave device, said master device comprising a transaction annotator for generating a transaction identifier as part of each transaction request passed from said master device to said first slave device, said transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request;

wherein said transaction identifier contains information enabling said first slave device to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from said master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers, wherein said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

99. (new) A master device operable to pass transaction requests across a common communication bus to a first slave device, said master device for providing a plurality of

communication paths between said master device, said first slave device and at least one further slave device, said master device comprising a transaction annotator for generating a transaction identifier as part of each transaction request passed from said master device to said first slave device, said transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request;

wherein said transaction identifier contains information enabling said first slave device to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from said master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers, wherein said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier, wherein said timeout value is derived from concatenated values of at least part of said master identifier portion and said priority portion of said transaction identifier.

100. (new) A first slave device operable to receive transaction requests from a master device across a common communication bus providing a plurality of communication paths between said master device, said first slave device and at least one further slave device, said first slave device having transaction ordering logic operable process a transaction identifier received from a master device as part of a transaction request, said transaction request having a master identifier portion and a priority request portion specifying a priority value for said transaction request, said transaction ordering logic being operable to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from said master identifier portions of

said transaction identifiers and in dependence upon said priority values of said transaction identifiers, said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

101 (new) A first slave device operable to receive transaction requests from a master device across a common communication bus providing a plurality of communication paths between said master device, said first slave device and at least one further slave device, said first slave device having transaction ordering logic operable process a transaction identifier received from a master device as part of a transaction request, said transaction request having a master identifier portion and a priority request portion specifying a priority value for said transaction request, said transaction ordering logic being operable to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from said master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers, wherein said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier, wherein said timeout value is derived from concatenated values of at least part of said master identifier portions and said priority portions of said transaction identifiers.

102. (new) A common bus carrying a transaction request signal from a master device to a first slave device, said common bus providing a plurality of communication paths between said master device, said first slave device and at least one further slave device, and for passing said

transaction request signal comprising a transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request, said transaction identifier enabling said first slave device to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers, wherein said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

103. (new) A common bus carrying a transaction request signal from a master device to a first slave device, said common bus providing a plurality of communication paths between said master device, said first slave device and at least one further slave device, and for passing said transaction request signal comprising a transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request, said transaction identifier enabling said first slave device to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers, wherein said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier, wherein said timeout value is derived from concatenated values of at least part of said master identifier portion and said priority portion of said transaction identifier.

104. (new) A data processing method for passing transaction requests from a master device to a slave device across a common communication bus providing a plurality of communication paths between said master device, said first slave device and at least one further slave device, said method comprising the steps of:

generating in a master device a transaction identifier as part of each transaction request passed from said master device to said first slave device, said transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request; and

determining at said first slave device an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers, wherein said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

105. (new) A data processing method for passing transaction requests from a master device to a slave device across a common communication bus providing a plurality of communication paths between said master device, said first slave device and at least one further slave device, said method comprising the steps of:

generating in a master device a transaction identifier as part of each transaction request passed from said master device to said first slave device, said transaction identifier having a

master identifier portion and a priority request portion specifying a priority value for said transaction request; and

determining at said first slave device an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers, wherein said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier, wherein said timeout value is derived from concatenated values of at least part of said master identifier portions and said priority portions of said transaction identifiers.

106. (new) A method of generating in a master device, transaction requests for sending across a common communication bus to a first slave device, said common communications bus providing a plurality of communication paths between said master device, said first slave device and at least one further slave device, said method comprising the step of:

generating a transaction identifier as part of each transaction request passed from said master device to said first slave device, said transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request;

wherein said transaction identifier contains information enabling said first slave device to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from said master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers, wherein said transaction ordering constraints are partially

derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

107. (new) A method of generating in a master device, transaction requests for sending across a common communication bus to a first slave device, said common communications bus providing a plurality of communication paths between said master device, said first slave device and at least one further slave device, said method comprising the step of:

generating a transaction identifier as part of each transaction request passed from said master device to said first slave device, said transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request;

wherein said transaction identifier contains information enabling said first slave device to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from said master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers, wherein said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier, wherein said timeout value is derived from concatenated values of at least part of said master identifier portion and said priority portion of said transaction identifier.

108. (new) A method of controlling a slave device to service transaction requests received from a master device across a common communication bus providing a plurality of communication paths between said master device, said first slave device and at least one further slave device, said method comprising the step of:

processing a transaction identifier received from a master device as part of a transaction request, said transaction request having a master identifier portion and a priority request portion specifying a priority value for said transaction request, said transaction ordering logic being operable to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from said master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers, wherein said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

109. (new) A method of controlling a slave device to service transaction requests received from a master device across a common communication bus providing a plurality of communication paths between said master device, said first slave device and at least one further slave device, said method comprising the step of:

processing a transaction identifier received from a master device as part of a transaction request, said transaction request having a master identifier portion and a priority request portion specifying a priority value for said transaction request, said transaction ordering logic being operable to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from said master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers, wherein said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction

identifier, wherein said timeout value is derived from concatenated values of at least part of said master identifier portions and said priority portions of said transaction identifiers.

110. (new) A method of transmitting a transaction request on a common communications bus providing a plurality of communication paths between a master device, a first slave device and at least one further slave device comprising the steps of:

generating a transaction request signal comprising a transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction request, said transaction identifier enabling said first slave device to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers; and

transmitting said transaction request signal across said common communication bus, wherein said transaction ordering constraints are partially derived from at least one of a request type of a transaction associated with said transaction identifier and a comparison of memory address ranges specified by said transaction requests.

111. (new) A method of transmitting a transaction request on a common communications bus providing a plurality of communication paths between a master device, a first slave device and at least one further slave device comprising the steps of:

generating a transaction request signal comprising a transaction identifier having a master identifier portion and a priority request portion specifying a priority value for said transaction

request, said transaction identifier enabling said first slave device to determine an order of service of a plurality of transaction requests having respective transaction identifiers in dependence upon transaction ordering constraints at least partially derived from master identifier portions of said transaction identifiers and in dependence upon said priority values of said transaction identifiers; and

transmitting said transaction request signal across said common communication bus, wherein said priority value is used to derive a timeout value for servicing of a transaction request associated with said transaction identifier, wherein said timeout value is derived from concatenated values of at least part of said master identifier portions and said priority portions of said transaction identifiers.